REMARKS/ARGUMENTS

In the Final action mailed June 1, 2007, claims 1, 3, 9, 10, and 16 were rejected and claims 2, 4- 8, 11 – 15, and 17 – 20 were objected to. Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims have been amended, added, or deleted.

Allowable Subject Matter

Applicants note with appreciation that claims 2, 4 – 8, 11 – 15, and 17 – 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants have chosen not to rewrite these claims at this time in view of the below-provided remarks.

Claim Rejections

Claim 1

Claim 1 recites:

> "One-time programmable memory device comprising an MOS (metal-oxide semiconductor) ***selection transistor*** and an MOS ***memory transistor*** connected in series between a voltage supply line and ground, and further comprising programming means for ***applying voltages*** to a gate of said selection transistor, ***to a gate of said memory transistor*** and to said voltage supply line, which applied voltages ***force said memory transistor into a snap-back mode*** resulting in a current thermally damaging a drain junction of said memory transistor." (emphasis added)

That is, the memory device includes a MOS selection transistor and a MOS memory transistor (referred to herein as simply the selection transistor and the memory transistor). Further, the memory device includes programming means for supplying voltages to a gate of the memory transistor to force the memory transistor into a snap-back mode.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fournel et al. (U.S. Pat. No. 5,943,264, hereinafter Fournel) in view of Tsukamoto (U.S. Pat. No. 6,298,459). In the Office action, the transistor T1/M1 of Fournel is cited for teaching the selection transistor and the PN semiconductor junction J1 of Fournel is cited for teaching "memory." The Office action admits that Fournel does not teach or

suggest that the memory is a MOS transistor but cites Tsukamoto as teaching the use of a MOS transistor as a PN diode.

Applicants assert that the combination of Fournel and Tsukamoto does not teach or suggest every limitation of claim 1. In particular, the prior art references do not teach or suggest a memory device having a selection transistor and a memory transistor in which a voltage is applied to a gate of the memory transistor to force the memory transistor into snap-back mode.

Fournel does not teach or suggest supplying voltages to ***a gate*** of a memory transistor

As stated above, transistor T1/M1 of Fournel is cited as teaching the selection transistor of claim 1 and the Office action admits that Fournel does not teach or suggest the memory transistor of claim 1. Although Fournel admittedly does not include a memory transistor, the Office action states that Fournel teaches "applying voltages…to a gate of said memory transistor." Applicants assert that it is impossible for Fournel to teach applying voltages "to ***a gate*** of said memory transistor" when Fournel admittedly does not teach or suggest a memory transistor. Further, Fournel cannot teach or suggest applying voltages "to a gate" of PN semiconductor junction J1 because PN semiconductor junction J1 does not have a gate. Because the Office action admits that Fournel does not include a memory transistor yet cites Fournel as teaching applying voltages "to a gate of said memory transistor," Applicants assert that a *prima facie* case of obviousness has not been established.

Fournel does not teach or suggest forcing a ***memory transistor*** into snap-back mode

The Office action identifies transistor T1/M1 as teaching the selection transistor in claim 1 and Fournel clearly teaches that the transistor T1/M1 is the transistor that is forced into snap-back mode. see Abstract, col. 2, line 28, col. 4, line 14, col. 7, line 5 In contrast to Fournel, claim 1 recites forcing the memory transistor into snap-back mode not the selection transistor. That is, Fournel teaches biasing only one transistor, transistor T1/M1, into snap-back mode and transistor T1 of Fournel is cited as teaching the selection transistor of claim 1 not the memory transistor. Applicants assert that Fournel cannot be cited for teaching transistor T1/M1 as both the selection transistor that is forced into snap-back mode and the memory transistor that is forced into snap-back mode. Further, it would not make sense for Fournel to

teach forcing the PN semiconductor junction J1 into snap-back mode because snap-back is a characteristic of a MOS transistor not a PN semiconductor junction. Additionally, Tsukamoto is cited merely for teaching a MOS transistor and does not teach or suggest that a memory transistor is forced into snap-back mode. Because Fournel teaches forcing the selection transistor into snap-back mode while claim 1 recites forcing the memory transistor into snap-back mode, Applicants assert that a *prima facie* case of obviousness has not been established.

Dependent Claims 3 and 9

Claims 3 and 9 depend from claim 1. Applicants assert that these claims are allowable at least based on an allowable claim 1.

Independent Claim 10

Claim 10 is a method claim that includes similar limitations to claim 1. Here, although the language of claim 10 differs from the language of claim 1 and the scope of claim 10 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to claim 1 apply also to claim 10. Accordingly, Applicants respectfully assert that independent claim 10 is not obvious from Fournel in view of Tsukamoto at least for similar reasons to those stated above in regard to independent claim 1.

Dependent Claim 16

Dependent claim 16 includes similar limitations to dependent claim 5. Dependent claim 16 is rejected in view of Fournel while claim 5 is deemed to be allowable. Applicants assert that claim 16 is allowable at least based on an allowable claim 10 or for similar reasons as claim 5.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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